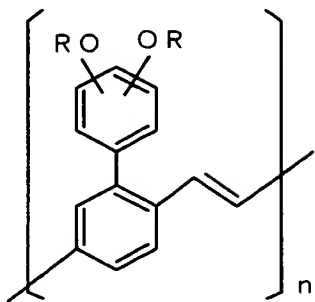
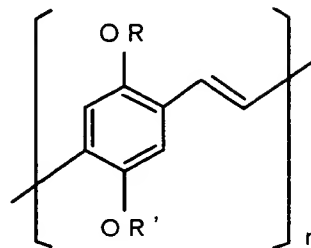


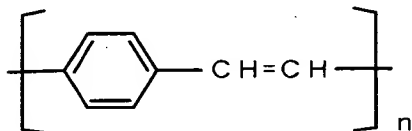
Compound 1



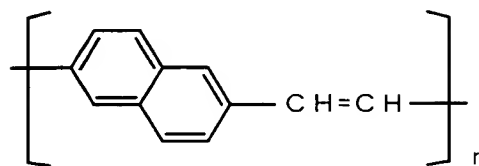
Compound 2



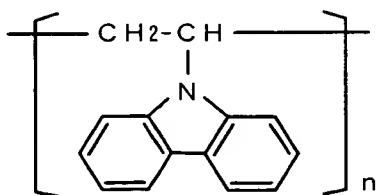
Compound 3



Compound 4



Compound 5



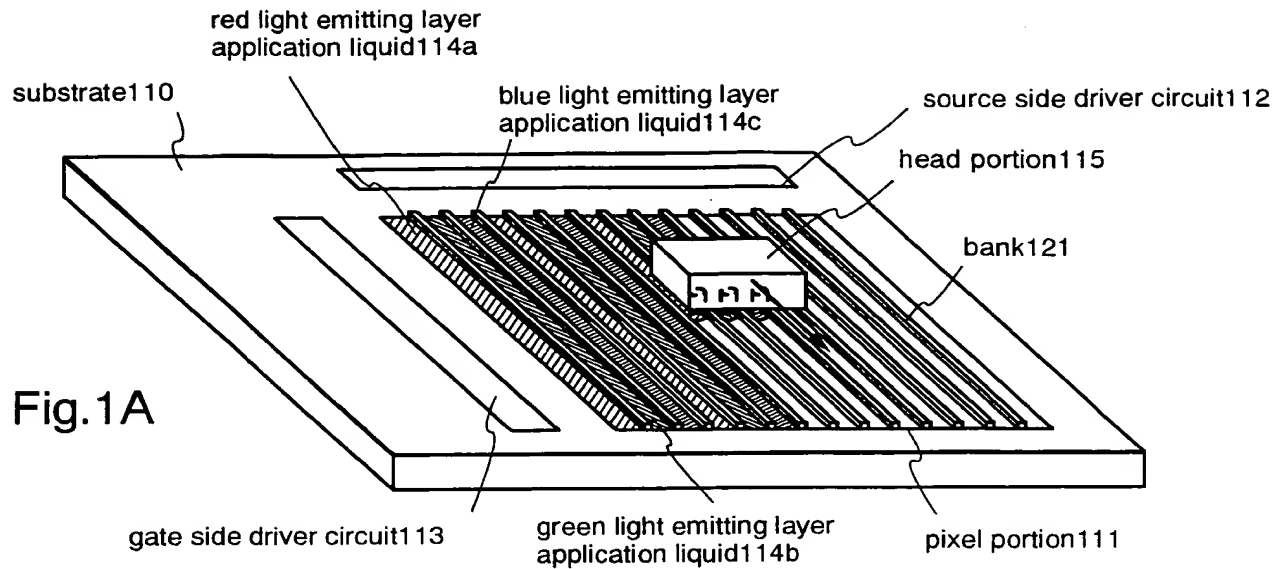


Fig. 1A

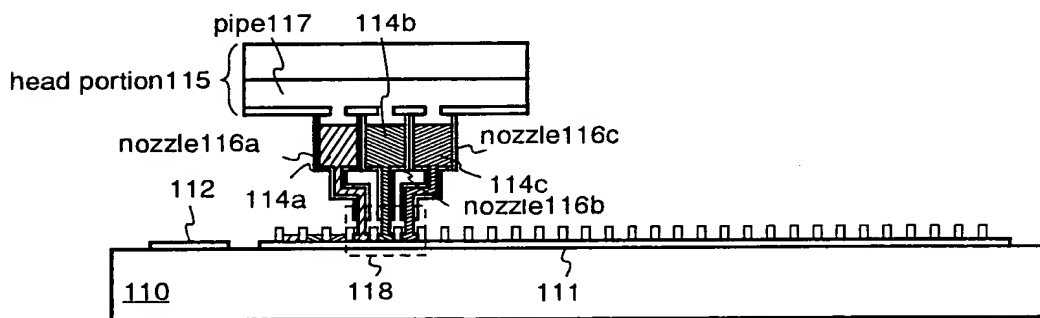


Fig. 1B

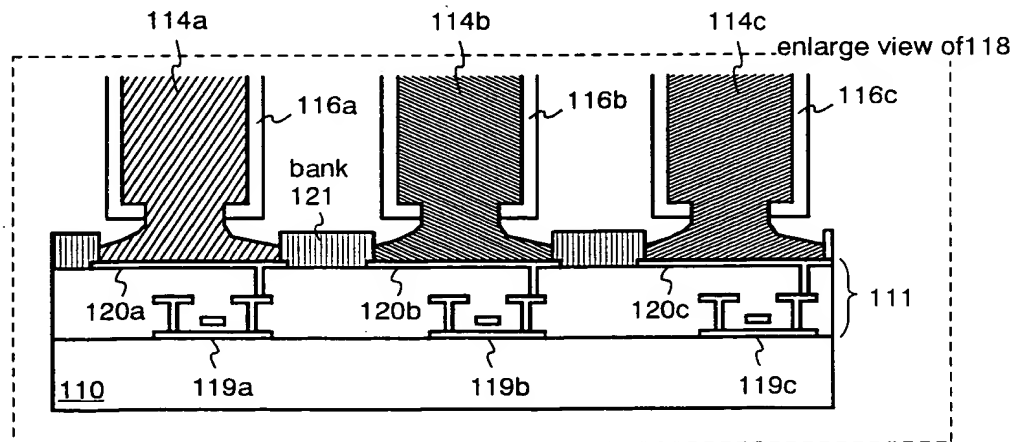
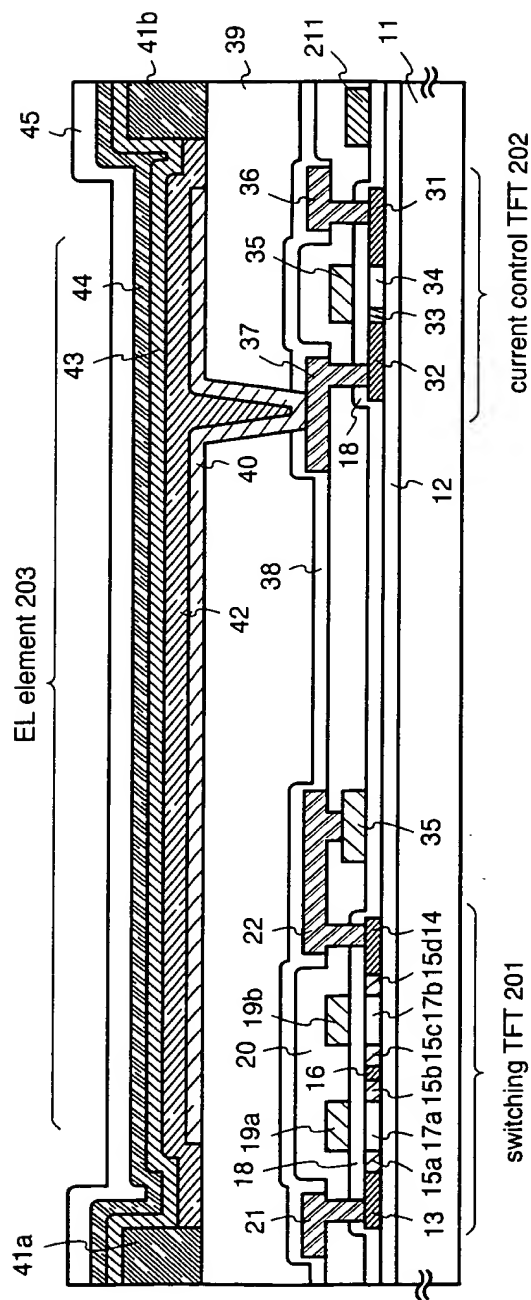


Fig. 1C



- 11: substrate 12: base film 13: source region 14: drain region 15a-15d: LDD regions
- 16: high concentration impurity regions 17a, 17b: channel forming region
- 18: gate insulating film 19a, 19b: gate electrodes 20: first interlayer insulating film
- 21: source wiring 22: drain wiring 23: gate electrode 31: source region 32: drain region
- 33: LDD region 34: channel forming region 35: gate electrode 36: source wiring
- 37: drain wiring 38: first passivation film 39: second interlayer insulating film
- 40: pixel electrode (cathode) 41: bank 42: light emitting layer 43: hole injection layer
- 44: anode 45: second interlayer insulating film

Fig. 2

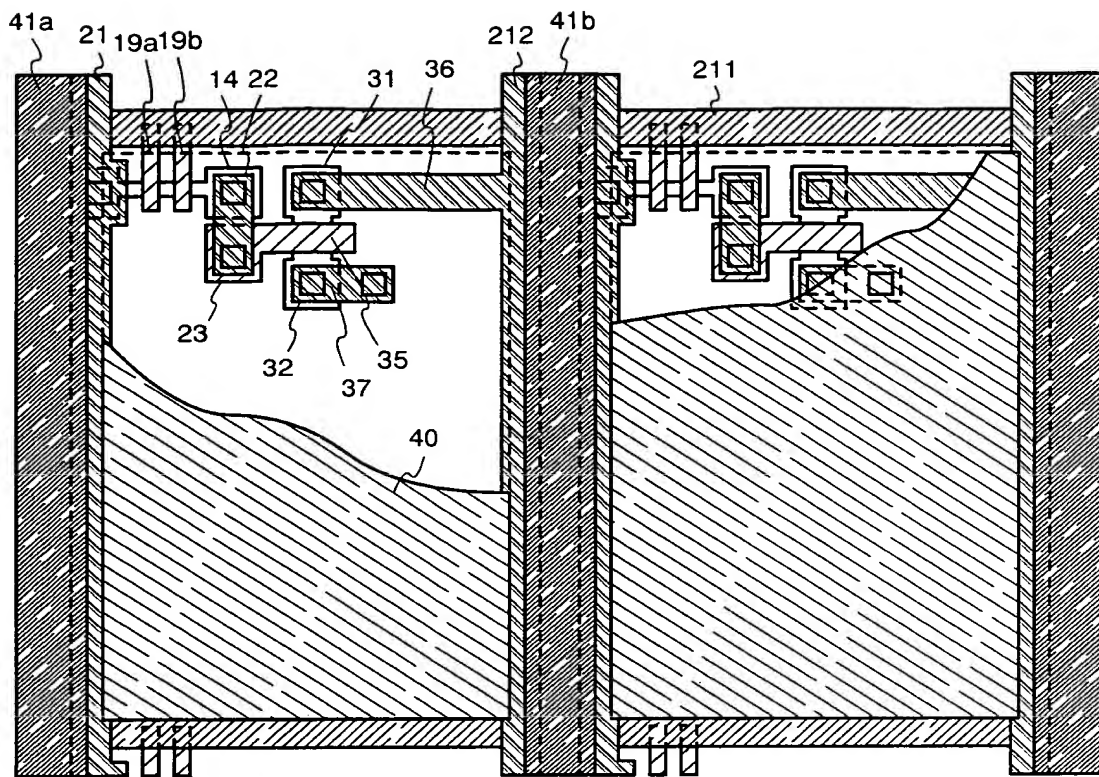


Fig.3A

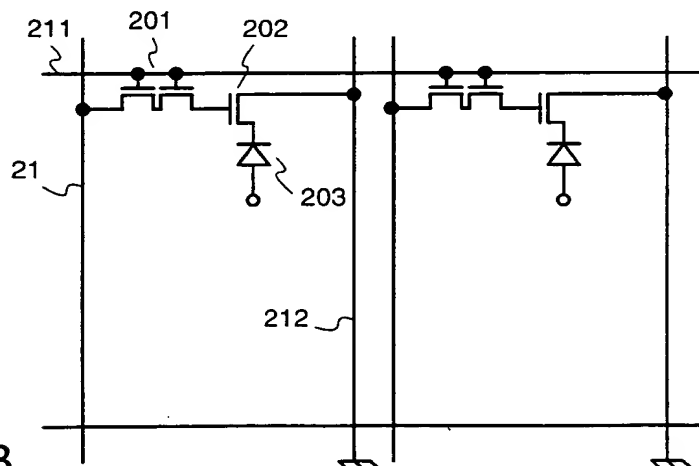
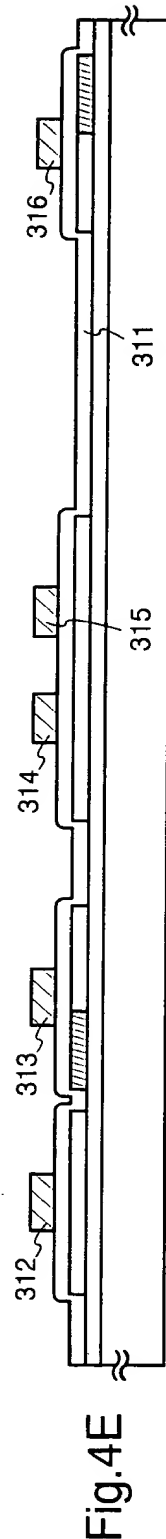
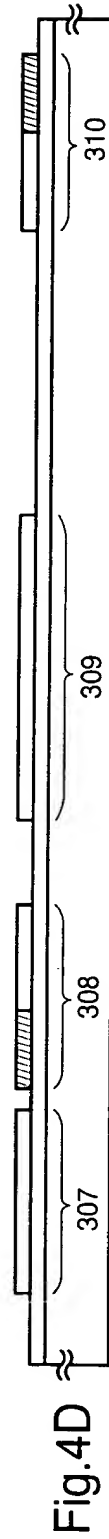
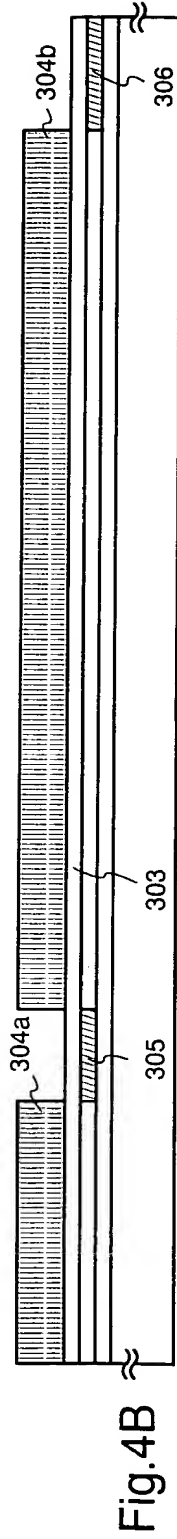
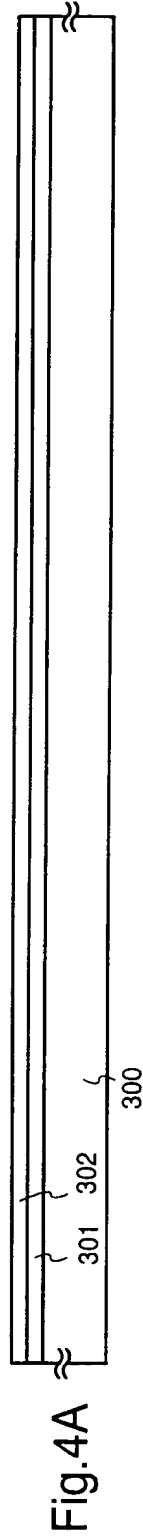


Fig.3B



300:glass substrate 301:base film 302:polysilicon film 303:protective film 304a-304b:resist mask  
305,306:n-type impurity regions 307-310:active layers 311:gate insulating film 312-316:gate electrodes

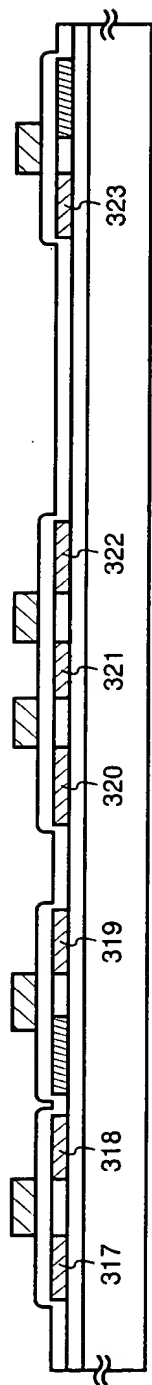


Fig.5A

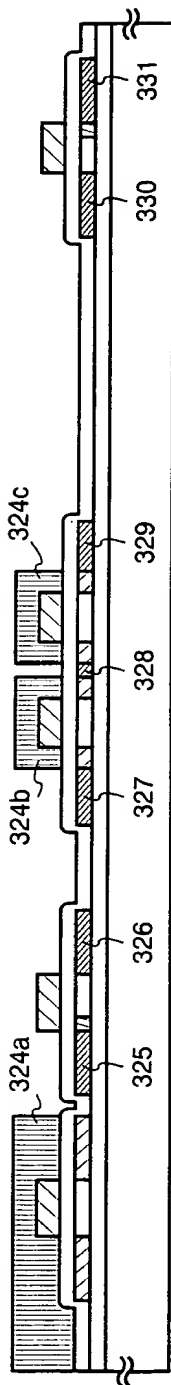


Fig.5B

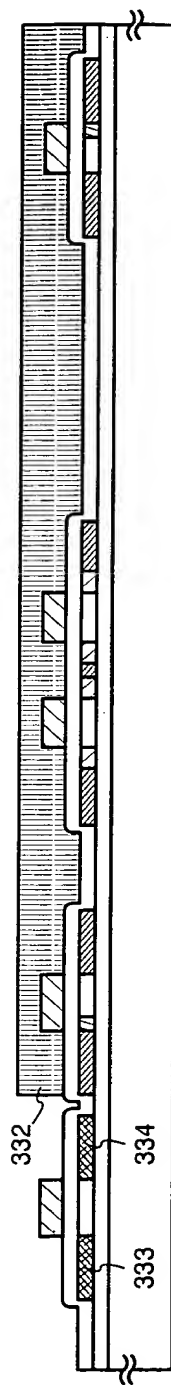


Fig.5C

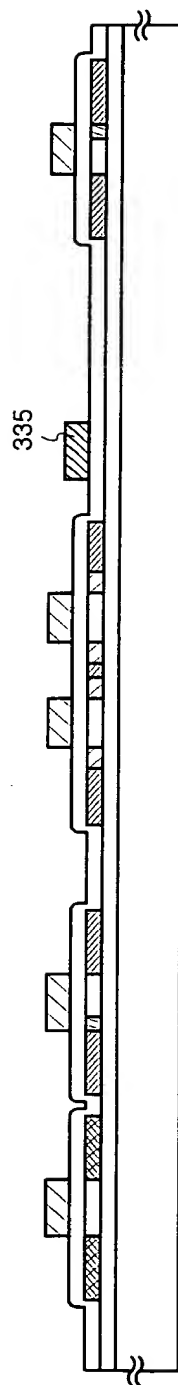


Fig.5D

317-323:n-type impurity regions 324a-324c,332:resist mask 325-331:n-type impurity regions  
 333,334:p-type impurity regions 335:gate wiring

FIG. 6A

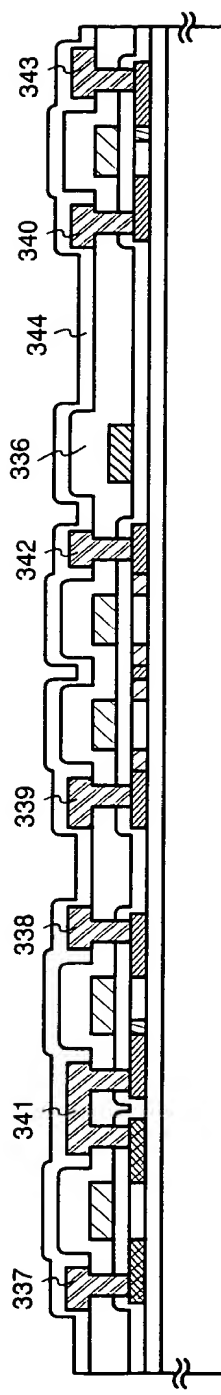


Fig.6A

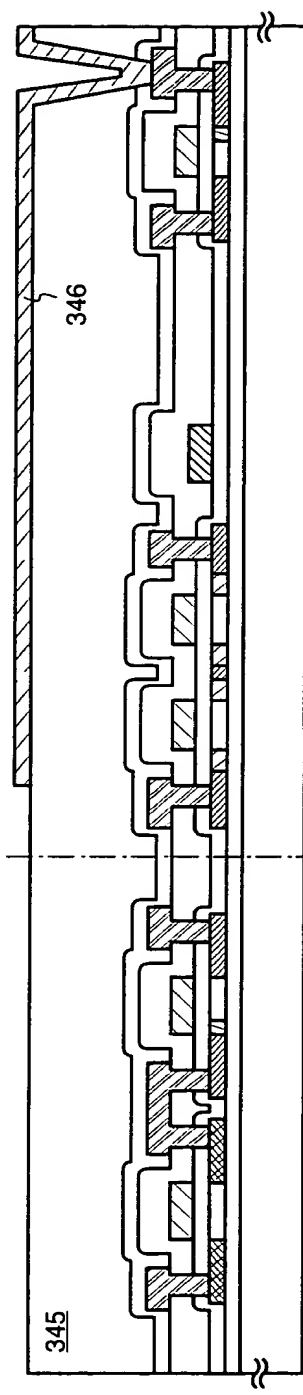


Fig.6B

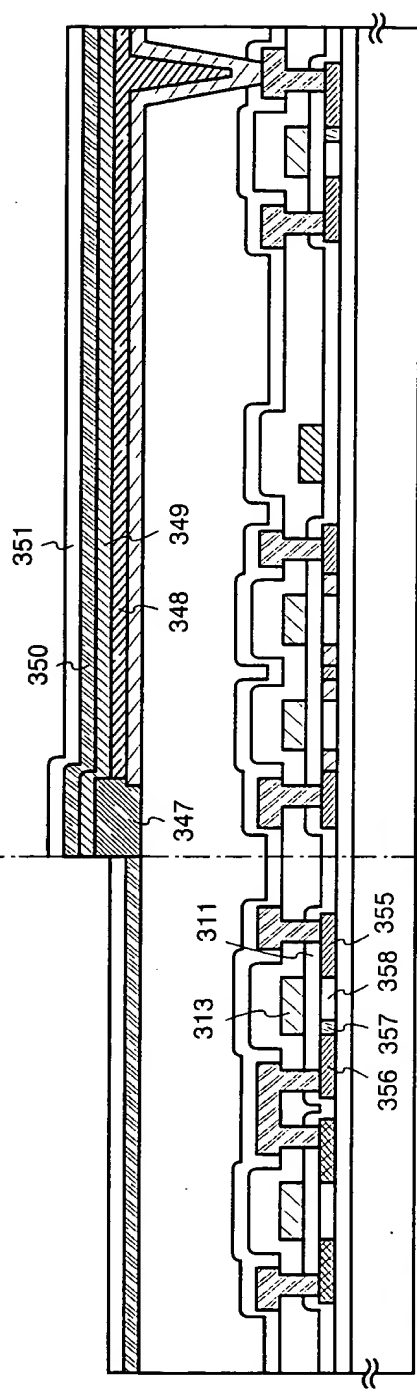
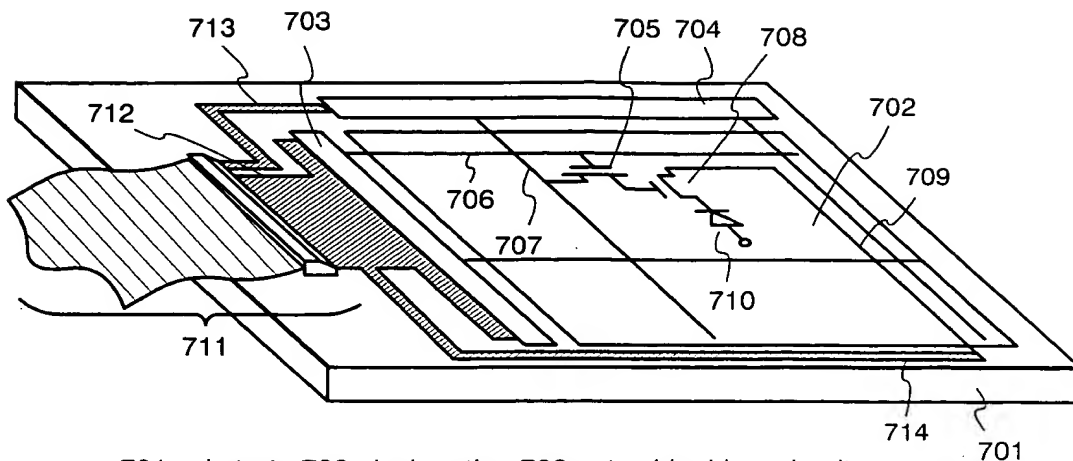


Fig.6C

p-channel type TFT206 n-channel type TFT205 switching TFT201 current control TFT202

336: first interlayer insulating film 337-340: source wiring 341-343: drain wiring  
 344: first passivation film 345: second interlayer insulating film 346: pixel electrode (cathode)  
 347: bank 348: light emitting layer 349: hole injection layer 350: anode 351: second passivation film



701:substrate 702:pixel portion 703:gate side driver circuit  
 704:source side driver circuit 705:switching TFT 706:gate wiring  
 707:source wiring 708:current control TFT 709:current supply line  
 710:EL element 711:FPC 712-714:connection wiring

Fig.7

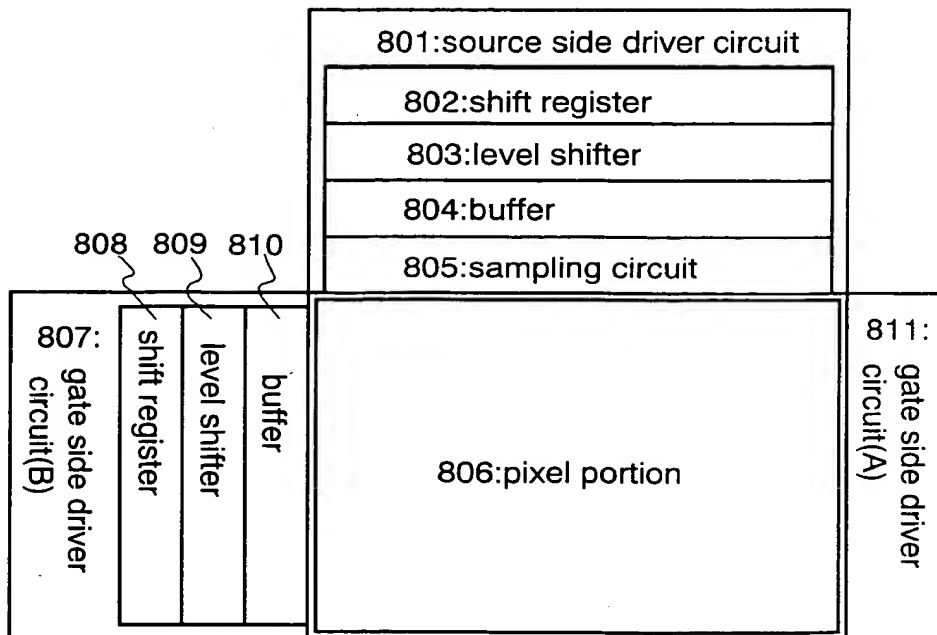


Fig.8



Fig.9

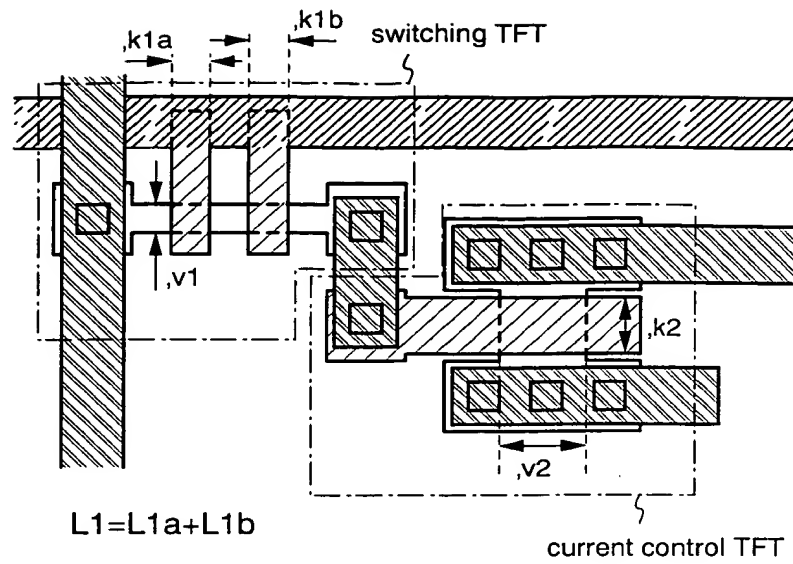
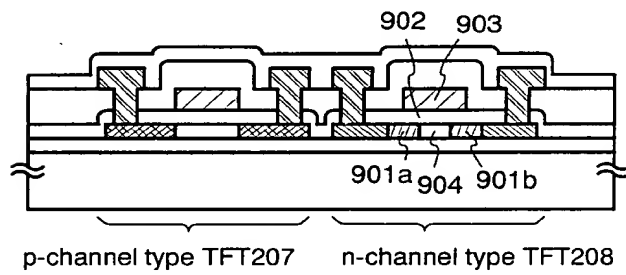


Fig.10



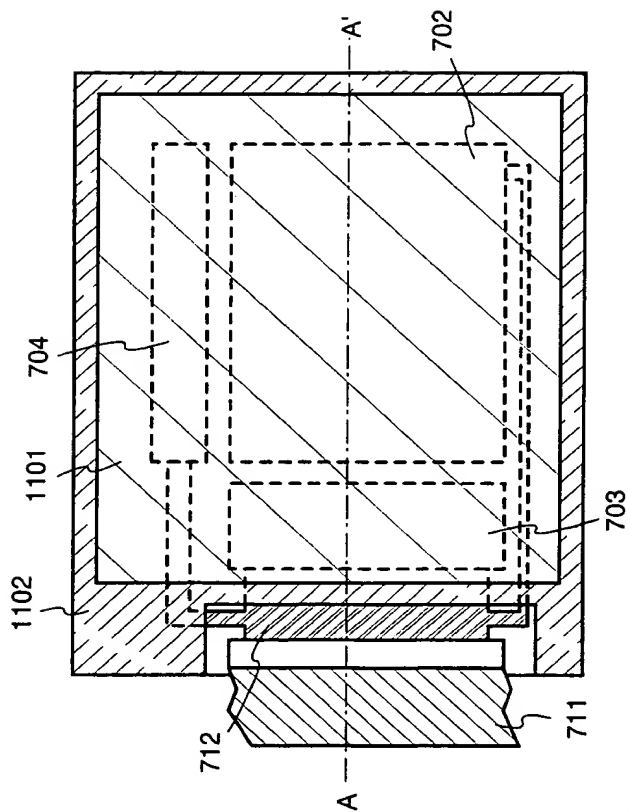


Fig.11A

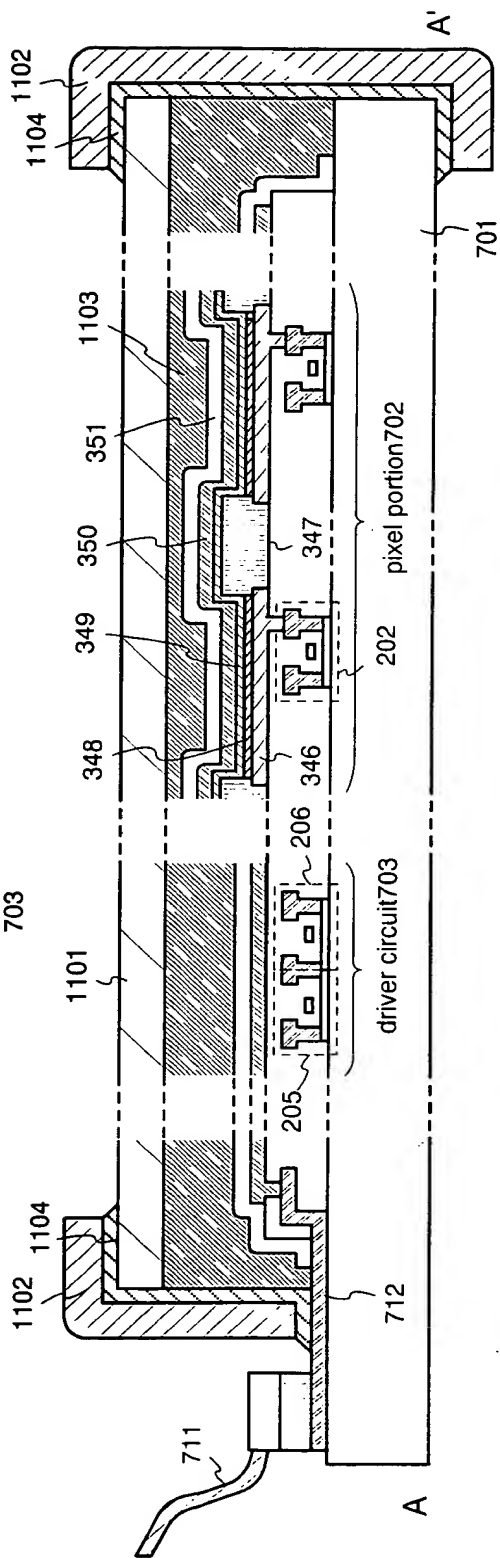


Fig.11B

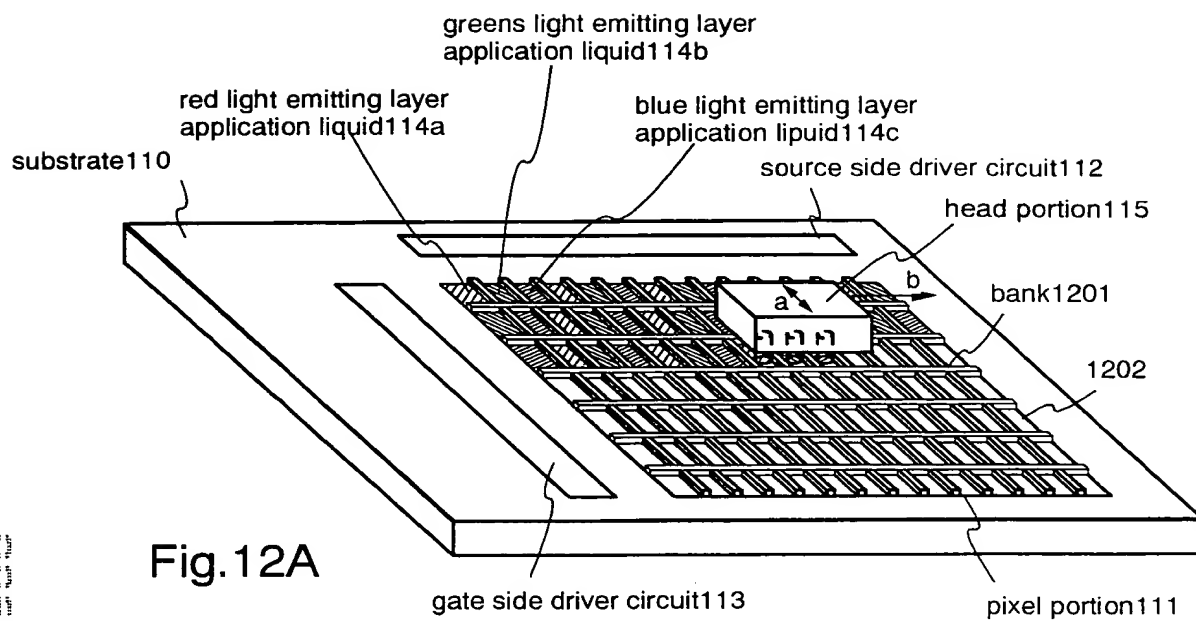


Fig.12A

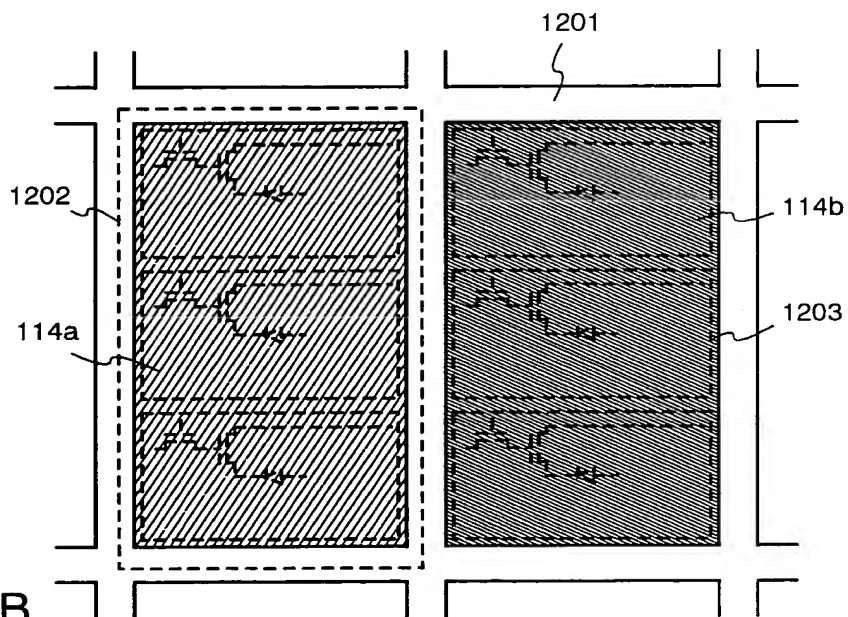


Fig.12B

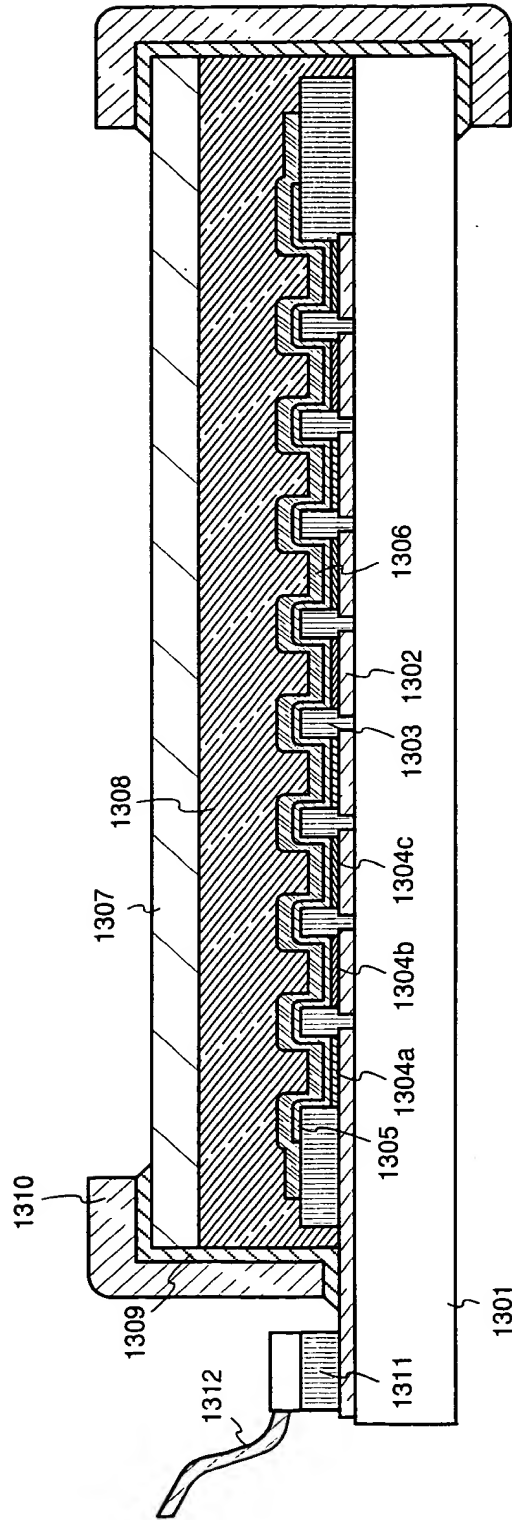


Fig.13

Fig.14A

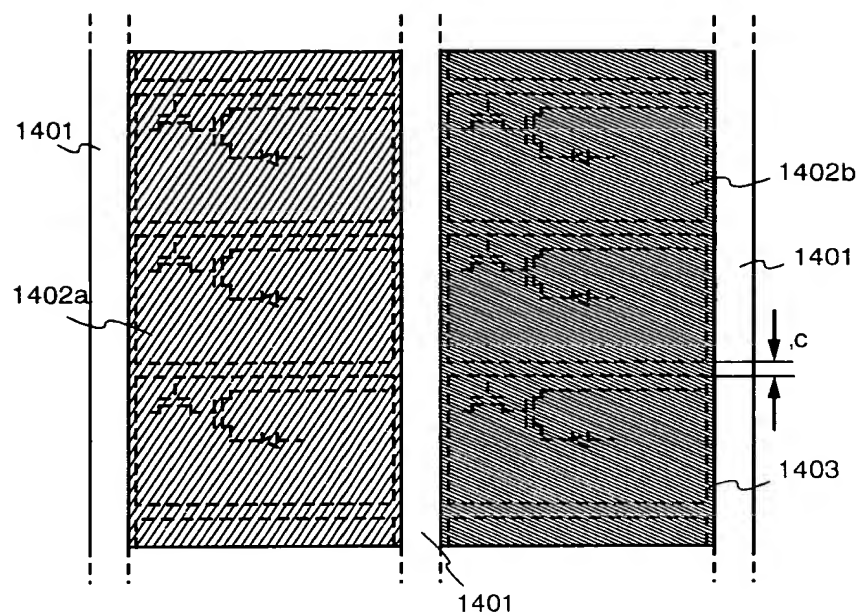


Fig.14B

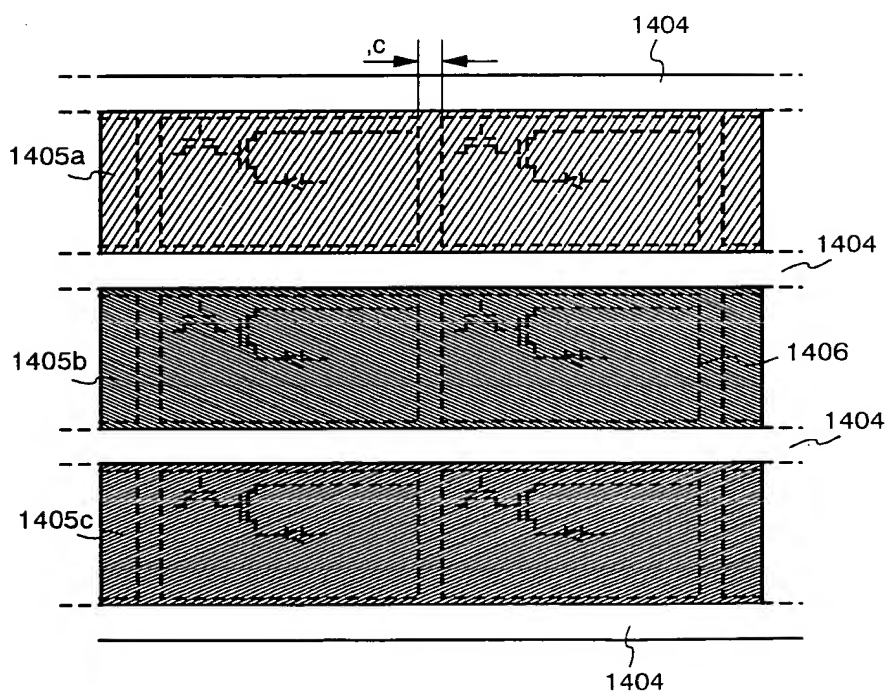


FIG. 15 is a cross-sectional view of a device 1300, showing a substrate 1301 with a series of conductive traces 1302. The traces are connected to a central conductive pad 1303. A dielectric layer 1304 is formed over the traces, with openings 1304a and 1304b. A conductive layer 1305 is formed in the openings. A conductive pad 1306 is formed over the central conductive pad 1303. A conductive pad 1307 is formed over the conductive layer 1305. A conductive pad 1308 is formed over the conductive layer 1305. A conductive pad 1309 is formed over the conductive layer 1305. A conductive pad 1310 is formed over the conductive layer 1305. A conductive pad 1311 is formed over the conductive layer 1305. A conductive pad 1312 is formed over the conductive layer 1305.

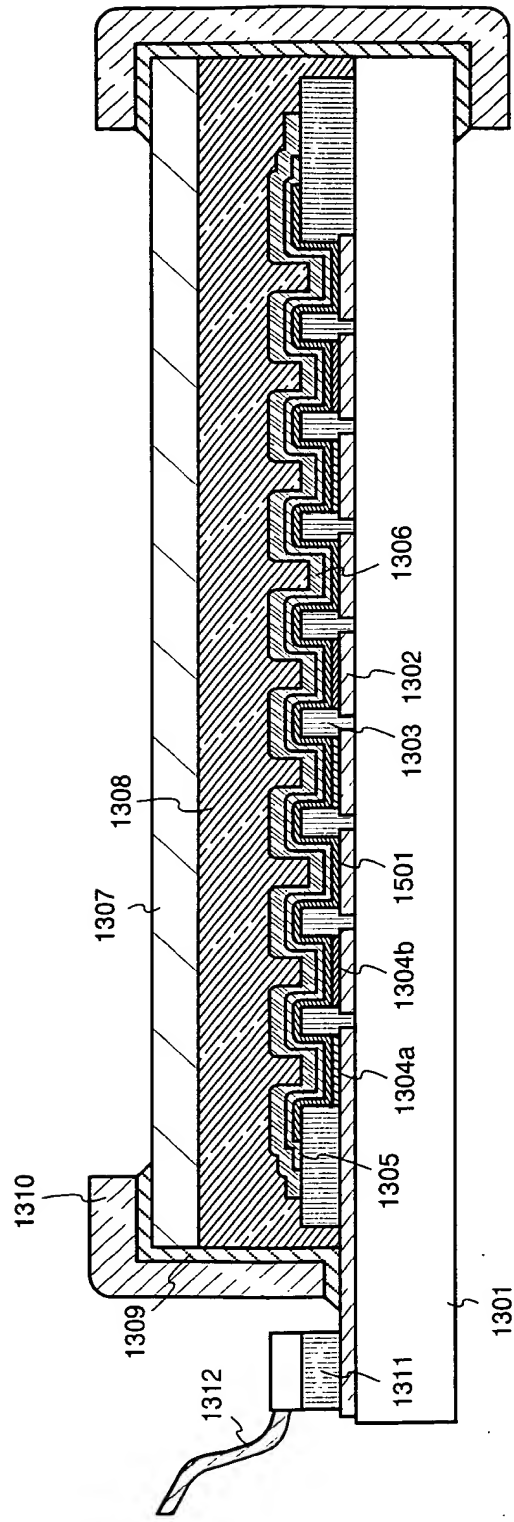


Fig.15

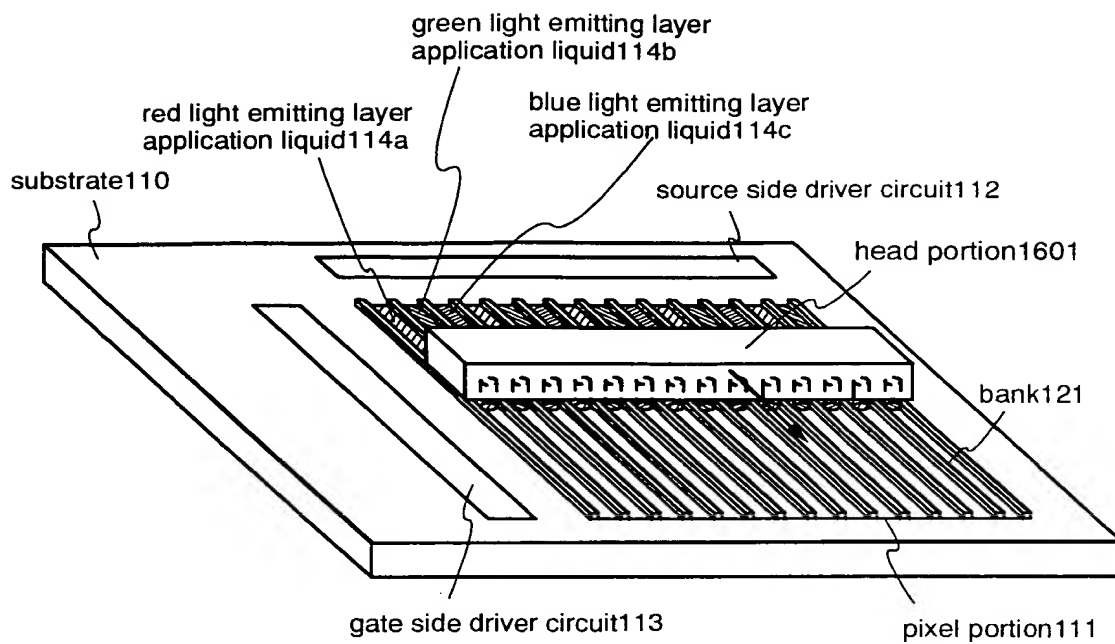


Fig.16

Fig.17A

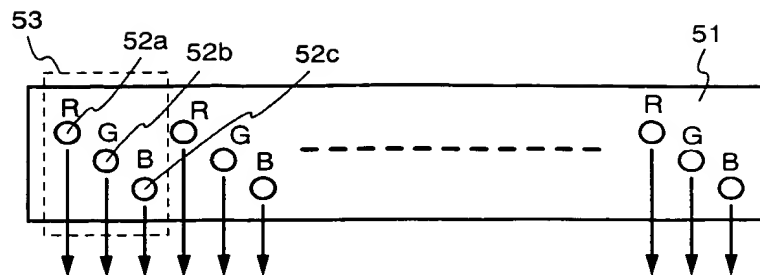


Fig.17B

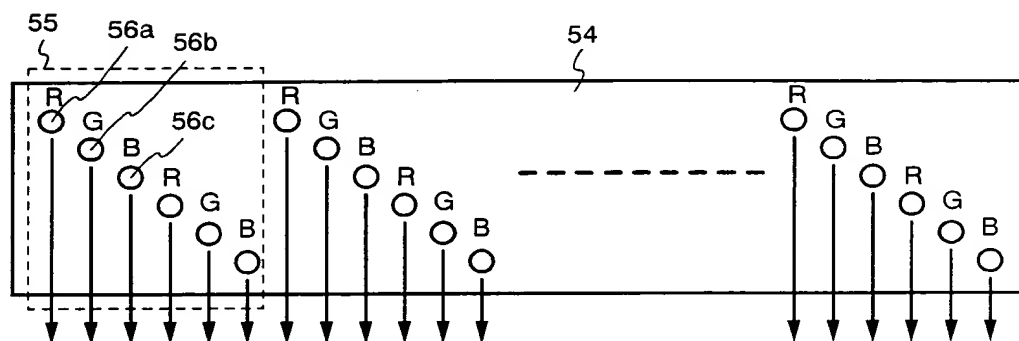
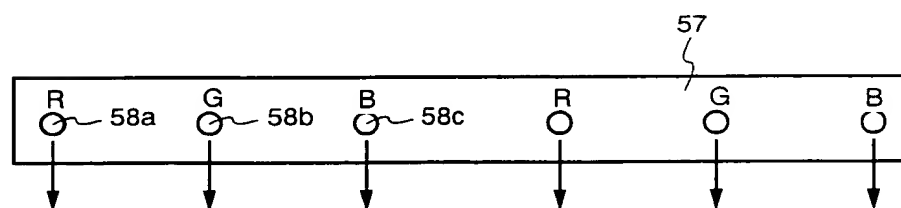


Fig.17C





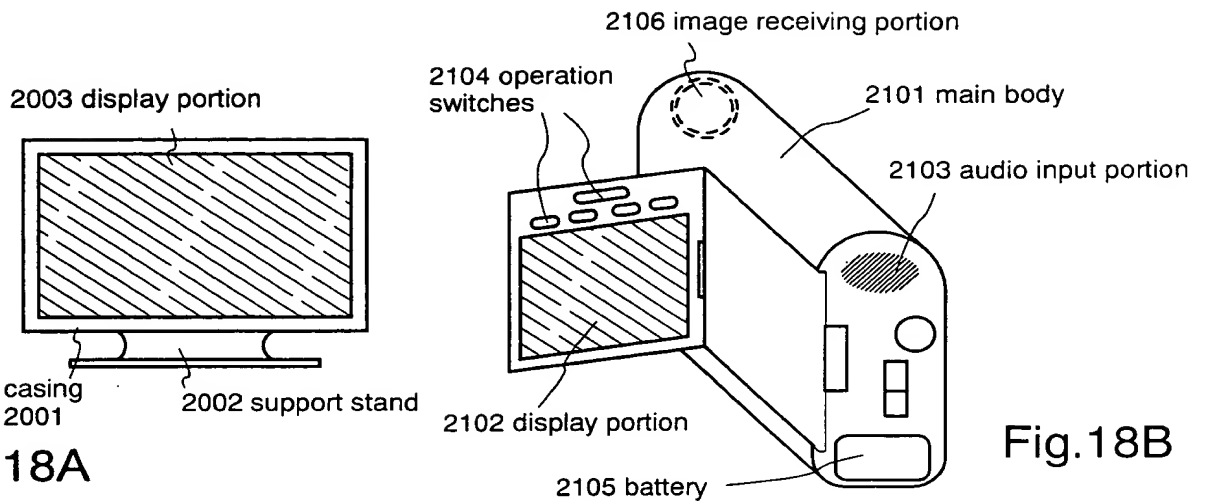


Fig.18A

Fig.18B

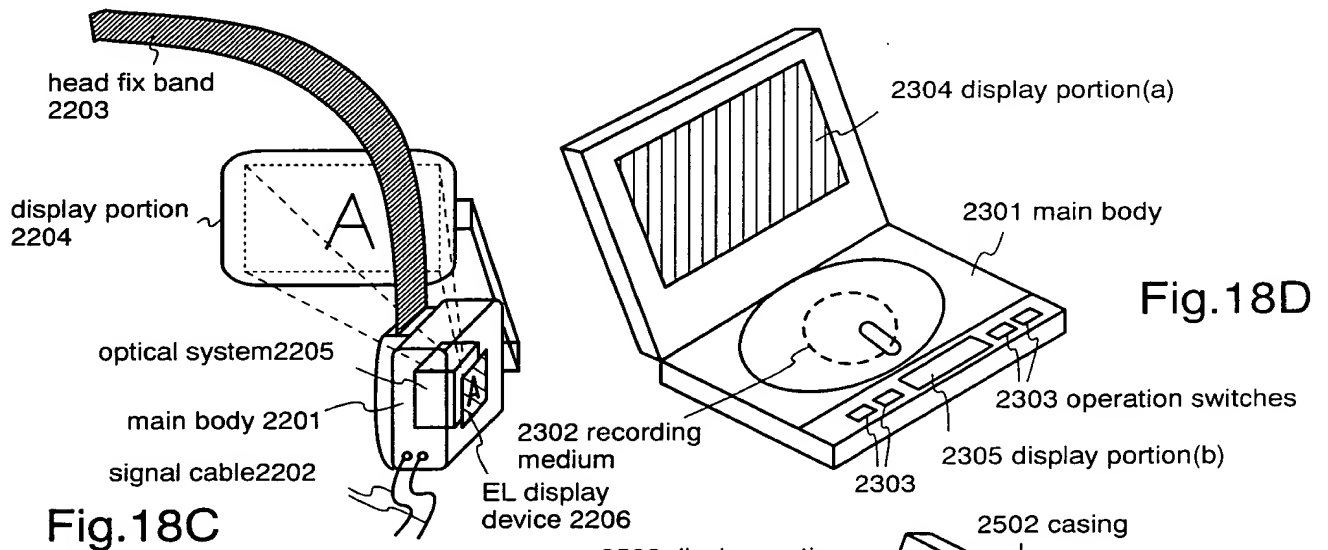


Fig.18C

Fig.18D

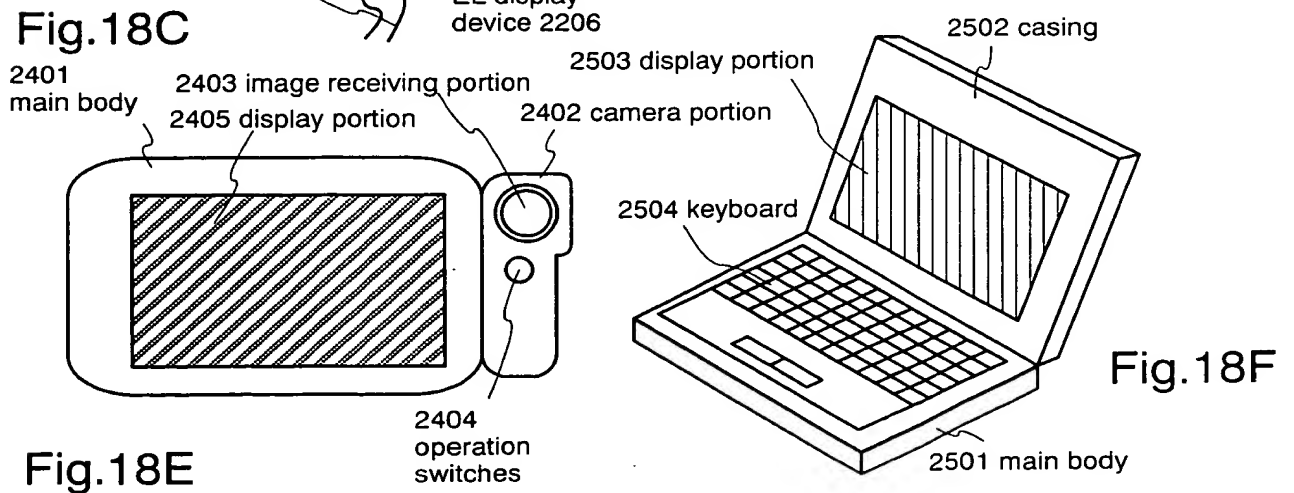


Fig.18E

Fig.18F

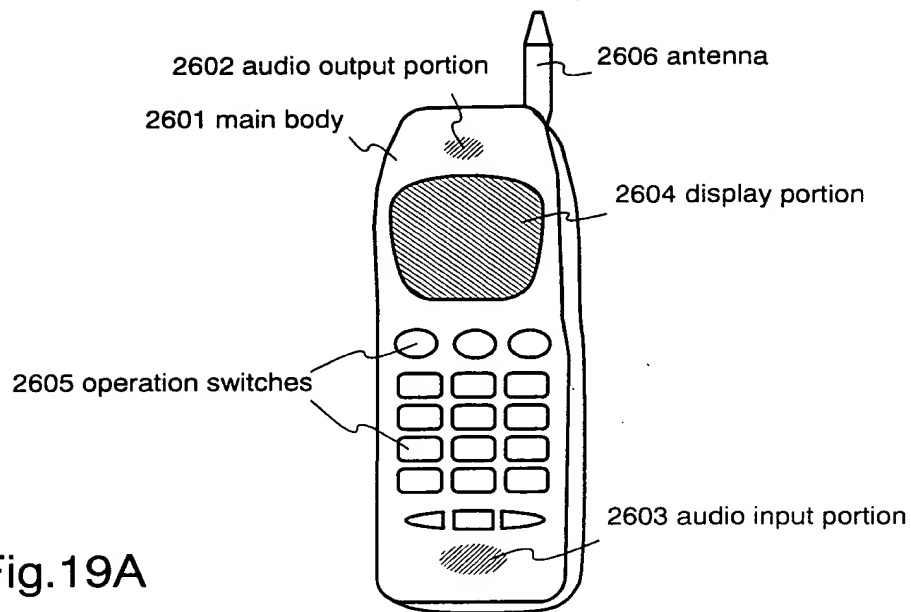


Fig.19A

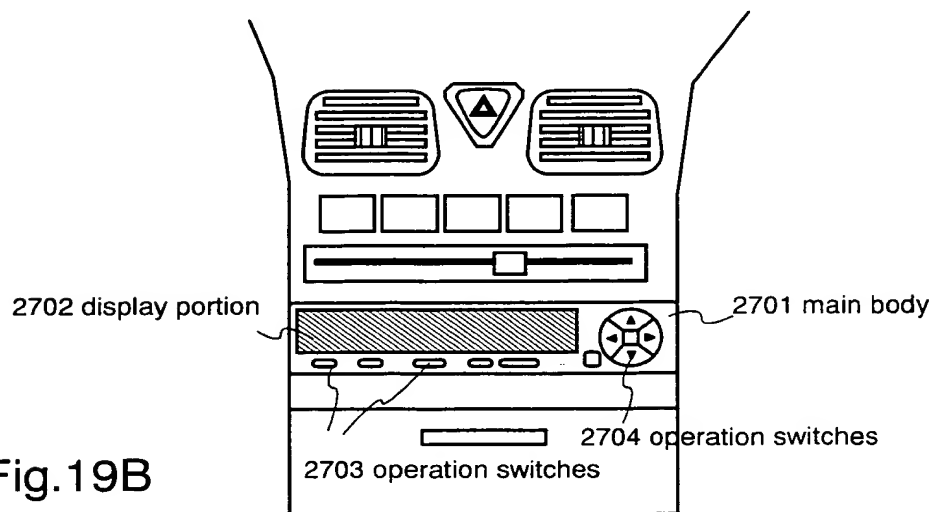


Fig.19B

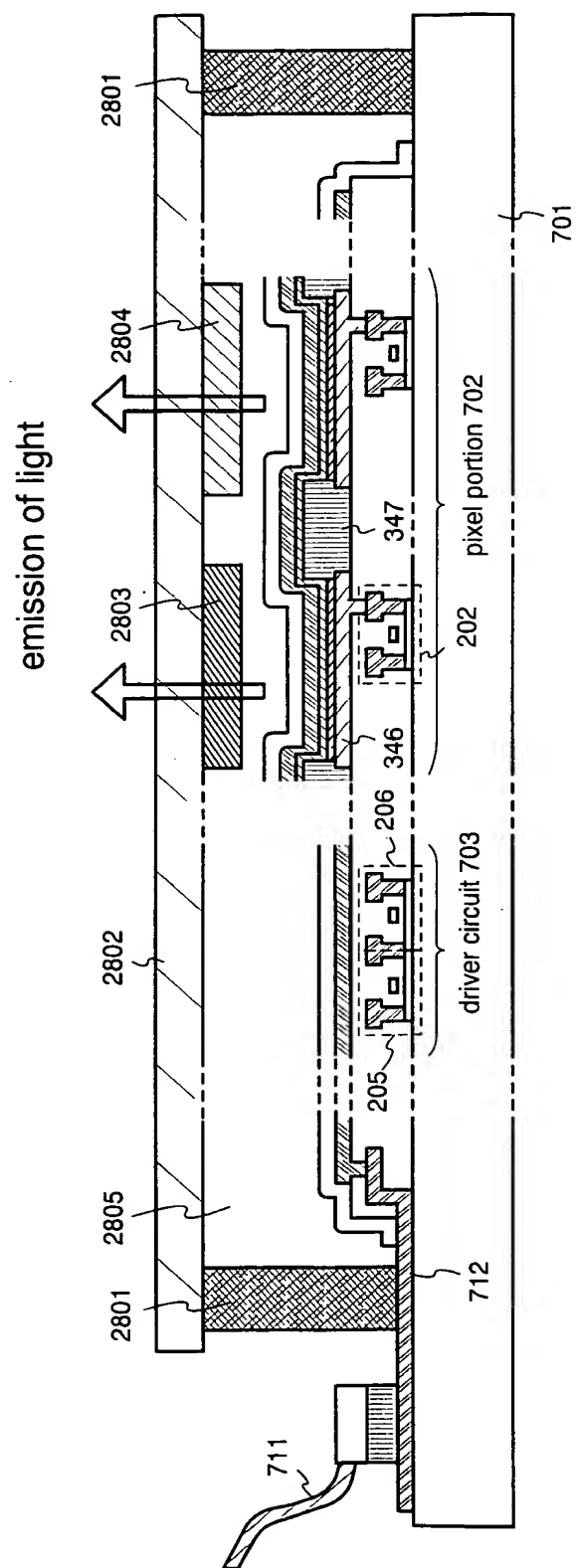


Fig.20

Fig.21A

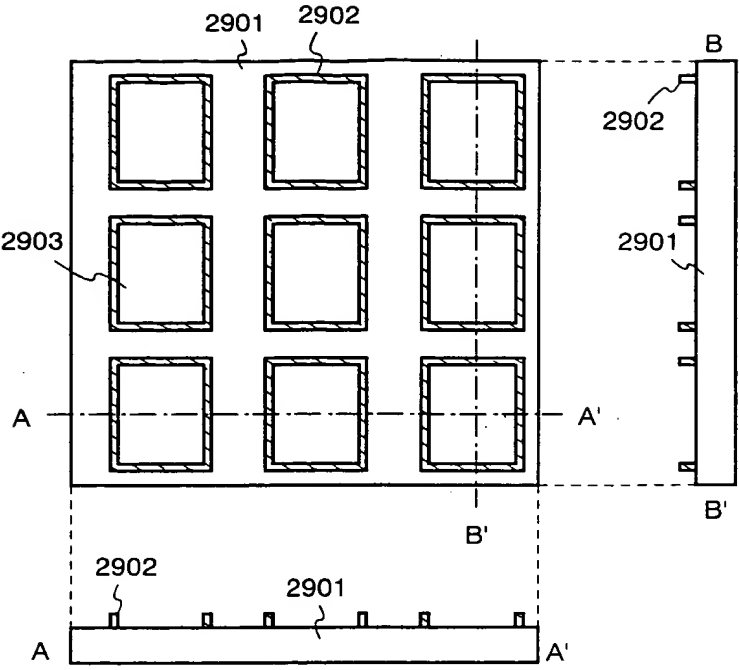


Fig.21B

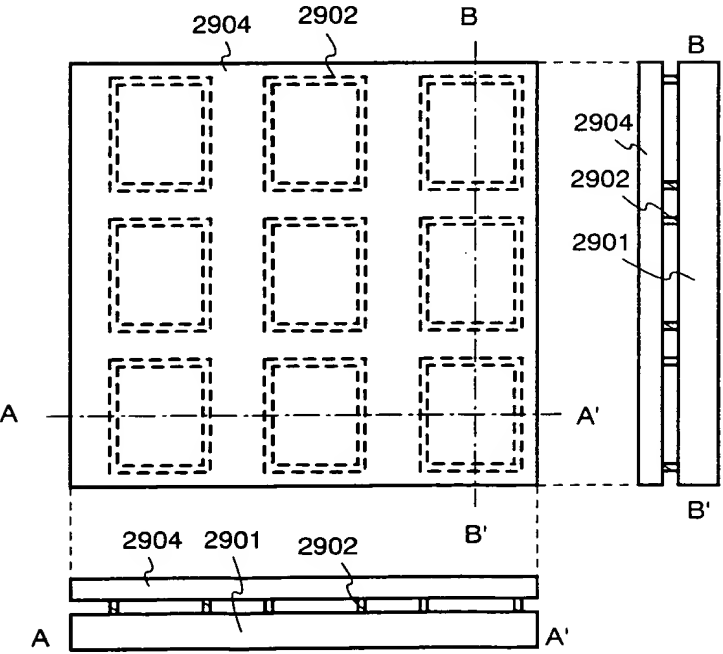


Fig.22A

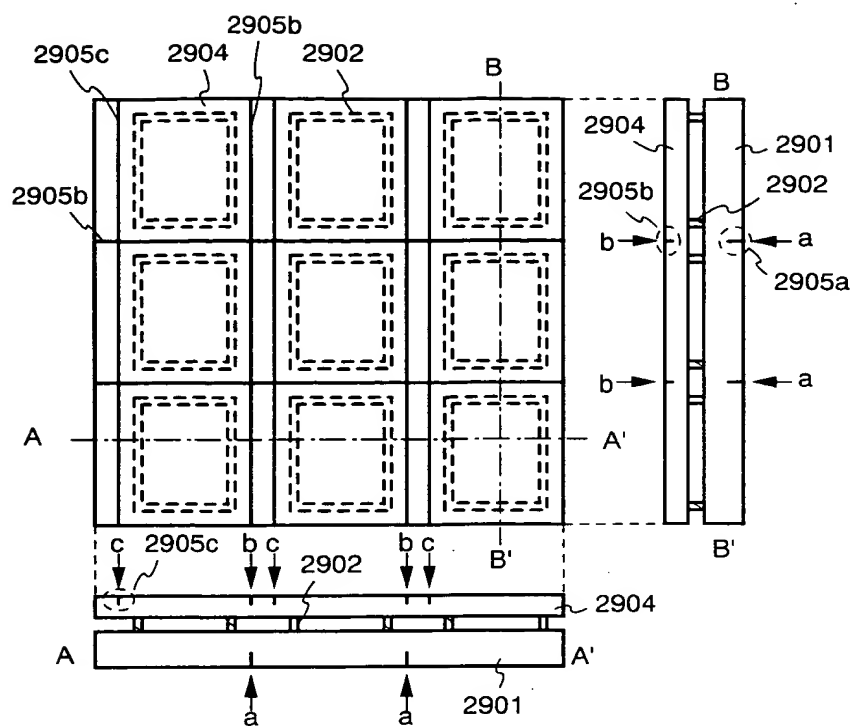
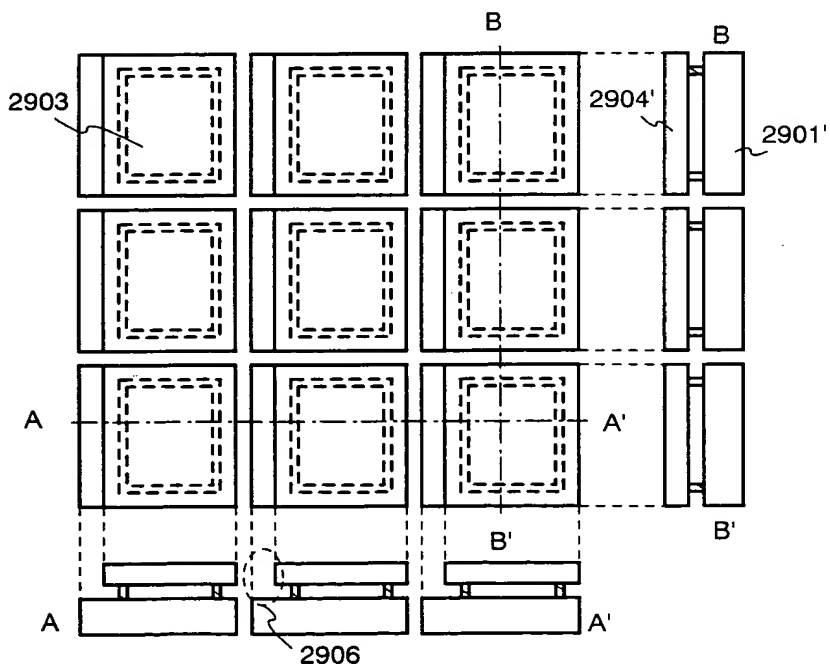


Fig.22B



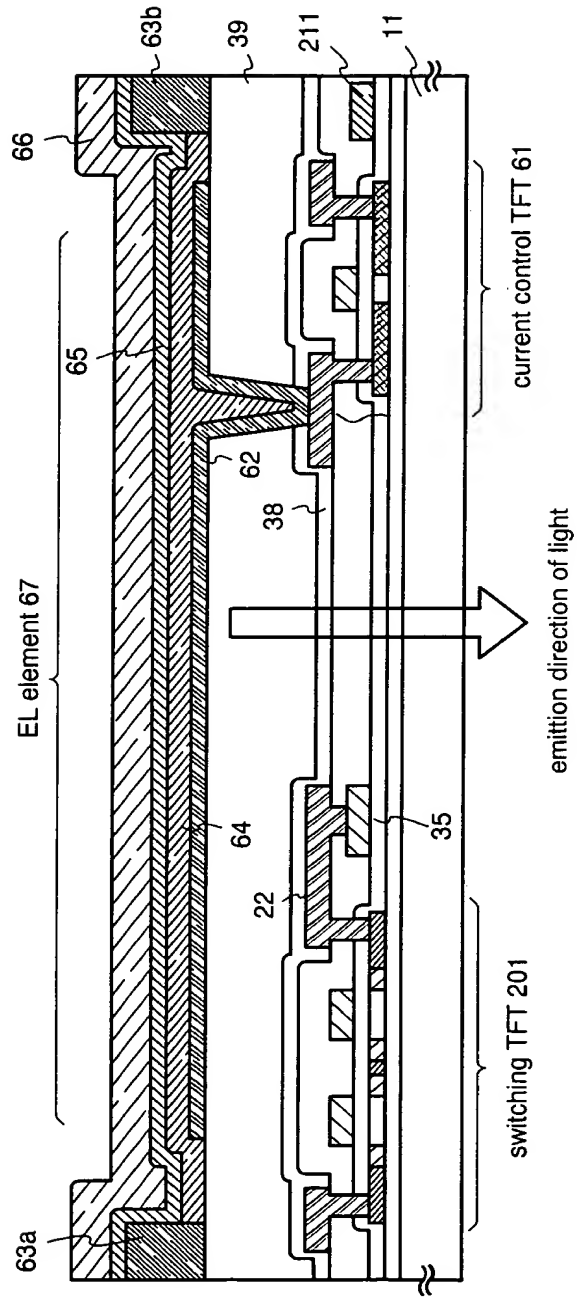


Fig.23

Fig.24A

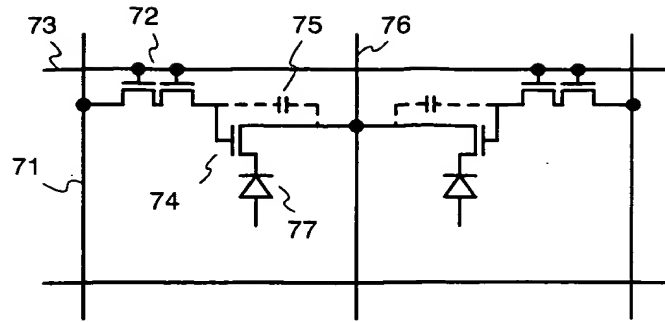


Fig.24B

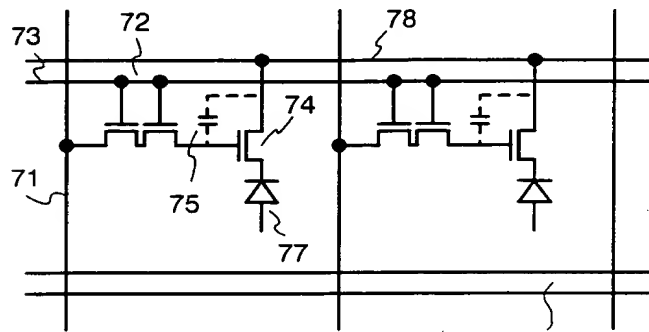


Fig.24C

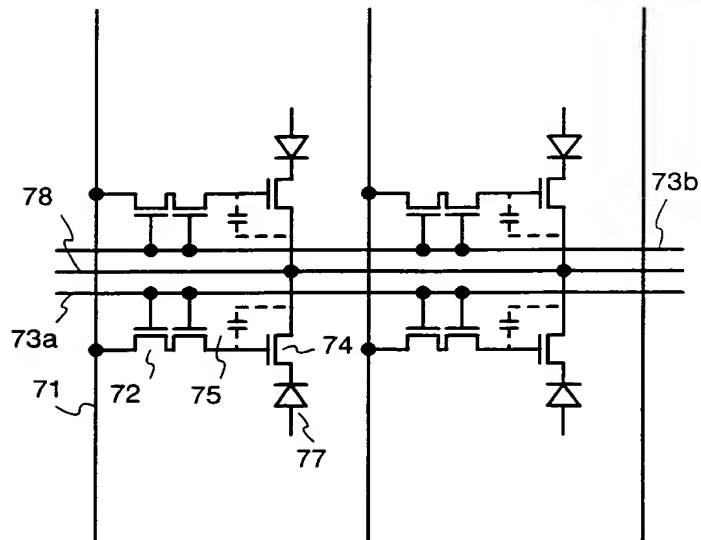


Fig.25A

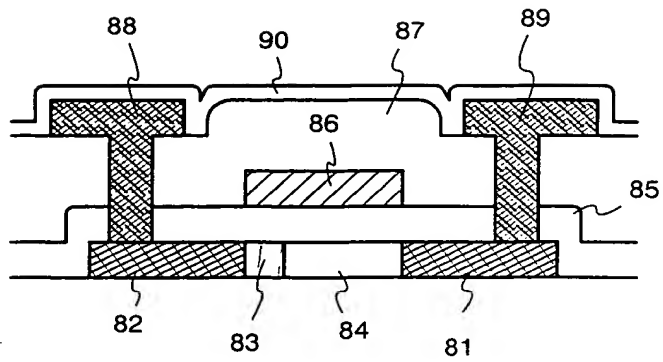


Fig.25B

